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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/726,220	11/28/2000	Farhad Fouladi	723-974	7835

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EXAMINER	
HSU, JONI	
ART UNIT	**PAPER NUMBER**
2628	

DATE MAILED: 03/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/726,220	FOULADI ET AL.	
	Examiner	Art Unit	
	Joni Hsu	2671	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-54 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-12,14,16-23,25,27-35,37,39,40,43-51,53 and 54 is/are rejected.

7)☒ Claim(s) 13,15,24,26,36,38,41,42 and 52 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's arguments with respect to claims 1-12, 14, 16-23, 25, 27-35, 37, 39, 40, 43-51, 53, and 54 have been considered but are moot in view of the new ground(s) of rejection.

2. Applicant's arguments, see pages 12-16, filed November 2, 2005, with respect to the rejection(s) of claim(s) 1-12, 14, 16-23, 25, 27-35, 37, 39, 40, 43-51, and 53 under 35 U.S.C. 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Chin (US006202101B1).

3. Applicant argues that the RWCQ 365 of Novak (US006295586B1) does not store requests for memory access, and therefore RWCQ 365 cannot constitute the multiple resource buffer memory of Claim 1 (page 13).

In reply, the Examiner agrees. However, new grounds of rejection are made in view of Chin.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 1-7, 14, 16-18, 25, 27-30, 37, 39, 40, 43-46, 53, and 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chin (US006202101B1) in view of Harriman (US006092158A).

7. With regard to Claim 1, Chin discloses in a graphics system including a main processor (12, Figure 1) and a graphics processing system (20) for generating graphics images on a display in cooperation with the main processor (Col. 1, lines 56-59; *CPU bus connects a CPU 12 to a bus interface unit 14, interface unit 14 may also include a graphics port to allow communication to a graphics accelerator 20*, Col. 7, lines 21-37), and a main memory (18), the system including

a plurality of resources (40, 42, 46, Figure 2) requesting access to the main memory, a memory controller comprising a plurality of buffer memories (50a, 50c, 50e, 50d, 50g, 50j, Figure 2), each of the buffer memories being operatively coupled to one of the plurality of resources requesting access to the main memory for storing information indicative of a request for main memory access (Col. 8, lines 20-37); a multiple resource buffer memory (memory request queue 68, Figure 6) coupled to the plurality of buffer memories for storing requests for main memory access from each of the plurality of resources; and a control circuit for controlling the transfer of information from the plurality of buffer memories to the multiple resource buffer memory (*temporarily stored within a M2P queue 50c*, Col. 12, lines 65-67; *type stored in the output pointer location within the in-order queue determines if the data at the head output pointer location is either read or write data, and thus whether the data is to be drawn from or sent to M2P or P2M (attributed to memory data queue), the memory request queue entry numbers are used to resolve snoop results maintained in the in-order queue 64*, Col. 13, line 51-Col. 14, line 5).

However, Chin does not disclose the means to reduce the frequency of switching from main memory write operations to main memory read operations. However, Harriman discloses separation of read and write access to optimize overall memory access times by grouping reads and writes to reduce bus turn around (*grouping reads and writes may also reduce "turn around"*, Col. 1, lines 35-50) similar to instant claim limitation "to reduce the frequency of switching from main memory write operations to main memory read operations".

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Chin to include the means to reduce the frequency of switching

from main memory write operations to main memory read operations as suggested by Harriman because it results in an improved and optimized overall memory access performance.

8. With regard to Claim 2, Chin discloses that the plurality of buffer memories (50a, 50e, 50g, Figure 2) are main memory write queues (Col. 8, lines 20-37).

9. With regard to Claim 3, Chin discloses that the multiple resource buffer memory (68, Figure 4) is a main memory write queue (Col. 11, lines 9-20).

10. With regard to Claim 4, Chin discloses that the plurality of buffer memories (50a, 50e, 50g, Figure 2) are main memory write queues (Col. 8, lines 20-37), and wherein the multiple resource buffer memory (68, Figure 6) is a main memory write queue (Col. 11, lines 9-20), and wherein the control circuit (44, Figure 2) is operable to control the rate at which write requests are coupled to the multiple resource buffer memory from the plurality of buffer memories (*Memory controller 44 arbitrates among processor write, processor reads, peripheral writes, peripheral reads and refresh. Arbitration for each cycle is pipelined into the current memory cycle which ensures that the next memory address is available on the memory bus before the current cycle is complete*, Col. 8, lines 52-67; Col. 13, line 51-Col. 14, line 5).

11. With regard to Claim 5, Chin discloses that the plurality of buffer memories (50a, 50e, 50g, Figure 2) are main memory write queues and further including a plurality of main memory

read queues (50c, 50d, 50j), each read queue being operatively coupled to a resource (40, 42, 46) requesting to read information from the main memory (18, Figure 1) (Col. 8, lines 20-37).

12. With regard to Claim 6, Chin describes that the control circuit (44, Figure 2) includes arbitration circuitry for arbitrating requests for access to the main memory (18, Figure 1) (Col. 8, lines 56-62).

13. With regard to Claims 7, 18, 30, and 46, Chin describes that the arbitration circuitry is operable to control the frequency with which the requesting resources are enabled to participate in the arbitrating for main memory access (Col. 8, lines 56-67).

14. With regard to Claims 14, 25, and 37, Chin discloses that the plurality of buffer memories (50a, 50c, 50e, 50d, 50h, 50g, 50j, Figure 2) and the multiple resource buffer memory (68, Figure 5) are write request queues (Col. 8, lines 20-37; Col. 11, lines 9-20), and wherein a resource that is writing to main memory generates a flush signal for initiating the flushing of that resource's write request queue (de-queuing, Col. 13, lines 1-11).

15. With regard to Claim 16, Claim 16 is similar in scope to Claim 1, and therefore is rejected under the same rationale.

16. With regard to Claim 17, Claim 17 is similar in scope to Claim 1, and therefore is rejected under the same rationale.

17. With regard to Claims 27 and 43, the claim limitation stating delaying forwarding requests for memory access to reduce the frequency of switch between memory read states and memory write states; and granting requests for memory access is similar in scope to Claim 1 and is rejected under the same rationale.

18. With regard to Claim 28, Chin discloses storing requests in a multiple resource write queue (68, Figure 4; Col. 11, lines 9-20).

19. With regard to Claim 29, Claim 29 is similar in scope to Claim 28, and therefore is rejected under the same rationale.

20. With regard to Claims 39 and 53, Chin discloses that the step of granting requests includes the step of fulfilling requests for main memory access in the order requested (*maintains prior ordering of data sent to and returned from the memory*, Col. 1, lines 9-15).

21. With regard to Claim 40, Claim 40 is similar in scope to Claim 14, and therefore is rejected under the same rationale.

22. With regard to Claim 44, Claim 44 is similar in scope to Claim 28, and therefore is rejected under the same rationale.

23. With regard to Claim 45, Claim 45 is similar in scope to Claim 29, and therefore is rejected under the same rationale.

24. With regard to Claim 54, Claim 54 is similar in scope to Claim 1, and therefore is rejected under the same rationale.

25. Claims 8-12, 19-23, 31-35, and 47-51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chin (US006202101B1) and Harriman (US006092158A) in view of Jeddeloh (US006330647B1).

26. With regard to Claims 8, 19, 31, and 47, Chin and Harriman are relied upon for the teachings as discussed above relative to Claim 1.

However, Chin and Harriman do not teach a memory access control register associated with one of the resources, wherein the control circuit includes arbitration circuitry responsive to the contents of the memory access control register for determining the frequency that the resource is permitted to participate in the arbitrating for main memory access. However, Jeddeloh discloses an arbiter 210 in combination with configuration registers 214 to record access count values for each requestor (resources or class of requester) and counters 214 may be used by arbiter 210 to track the number of memory access operations remaining for a selected requester (Col. 3, lines 53-67; Col. 4, lines 1-30).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the devices of Chin and Harriman to include a memory access control

register associated with one of the resources, wherein the control circuit includes arbitration circuitry responsive to the contents of the memory access control register for determining the frequency that the resource is permitted to participate in the arbitrating for main memory access as suggested by Jeddeloh because it provides for efficient memory access control without denying access to those requestors issuing single access transactions and/or low priority requests for an unacceptable long time (Col. 1, lines 48-51).

27. With regard to Claims 9, 20, 32, and 48, Chin does not teach a set of control registers, the control registers being programmable by the main processor. However, Jeddeloh discloses the control registers (configuration registers 212) being programmable by the main processor (system controller 102) (*system controller 102...may...set and adjust requestor access count values...(i.e., modify values stored in configuration register 212*, Col. 5, lines 1-10). This would be obvious for the same reasons given in the rejection for Claim 8.

28. With regard to Claims 10, 21, 33, and 49, Chin discloses that the control circuitry (44, Figure 2) is operable to arbitrate between the resources for granting requests for main memory access (Col. 8, lines 56-62).

However, Chin does not teach wherein the control registers include a plurality of memory bandwidth control registers which are accessed by the control circuitry in determining which resource will be granted main memory access. However, Jeddeloh discloses implicitly, wherein the control registers include a plurality of memory bandwidth control registers which are accessed by the control circuitry in determining which resource will be granted main memory

access (*count values may be determined dynamically at...system start up and/or modified during system operations...access count values may be based on requestor operating speed, wherein faster devices are allocated larger access count values*, Col. 5, lines 1-10). This would be obvious for the same reasons given in the rejection for Claim 8.

29. With regard to Claims 11, 22, 34, and 50, Chin does not teach that each of the memory bandwidth control registers is respectively associated with a resource seeking main memory access. However, Jeddeloh discloses wherein each of the memory bandwidth control registers (configuration registers 212) is respectively associated with a resource seeking main memory access (*configuration registers 212 may be used to record access count values for each requestor (or class of requestor)*, Col. 4, lines 1-6). This would be obvious for the same reasons given in the rejection for Claim 8.

30. With regard to Claims 12, 23, 35, and 51, Chin does not teach that the control registers include at least one register associated with a main memory access requesting resource for storing data for the requesting resource indicative of at least one of memory usage and memory bandwidth for that resource. However, Jeddeloh discloses implicitly at least one register for the requesting resource indicative of at least one of memory usage and memory bandwidth for that resource (*configuration registers 212 may be used to record access count values...counters 214 may be used by arbiter 210 to track number of memory access operations*, Col. 4, lines 1-6). This would be obvious for the same reasons given in the rejection for Claim 8.

Allowable Subject Matter

31. Claims 13, 24, 36, and 52 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Prior art fails to particularly disclose a register indicative of wasted memory cycles due to granting memory access to that resource.

32. Claims 15, 26, 38, 41, and 42 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joni Hsu whose telephone number is 571-272-7785. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ulka Chauhan can be reached on 571-272-7782. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JH

ULKA CHAUHAN
SUPERVISORY PATENT EXAMINER